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[MEMORY DEVICE STRUCTURE AND METHOD OF FABRICATING THE SAME]

Abstract

A method of fabricating a memory device structure, where the method includes the steps of forming a tunnel oxide layer, a silicon nitride layer and a silicon oxide layer. A conductive layer is then formed on top of the silicon oxide. The conductive layer is then patterned to form a conductive gate layer. The silicon oxide layer is patterned during the same step of patterning the conductive layer, exposing the silicon nitride layer. Following that, a blanket dielectric layer is then formed on the substrate. This blanket dielectric layer is patterned with one etch step to form a spacer wall at the sides of the conductive gate layer.